SONY

CXA1385Q

LCD TV YC Jungle

T-77-29

Description

The CXA1385Q is a LCD TV IC that converts the composite video signals to RGB equivalents. It is ideally suited for use in a 2- to 4-inch LCD TV set. It incorporates all filters necessary for signal processing.

32 pin QFP (Plastic)

Features

- Built-in delay line (Y/C delay alignment)
- Built-in TRAP, BPF, and SHARPNESS functions
- Built-in APL circuit
- Few number of parts (approximately 50 parts)
- Low power consumption 135mV (Vcc=5V).

Absolute Maximum Ratings

• Supply voltage	Vcc	14	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	500	mW

Operating Conditions

Supply voltage	Vcc	4.75 to 5.25	V

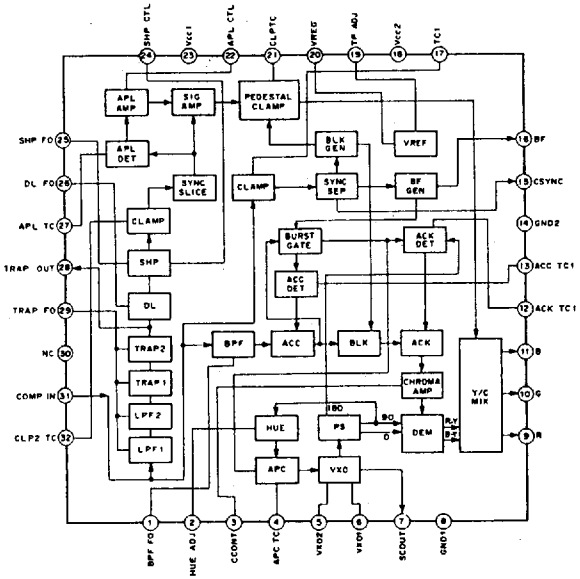
Applications

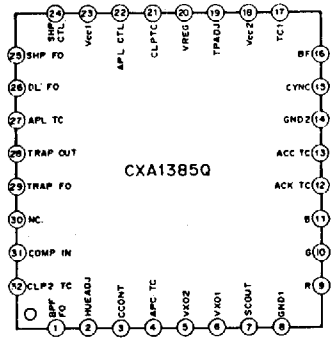
Color LCD TV sets etc.

Structure

Bipolar silicon monolithic IC

Block Diagram and Pin Configuration





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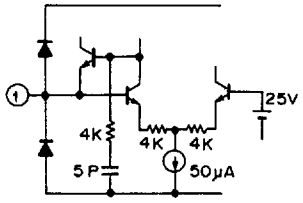
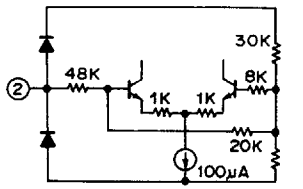
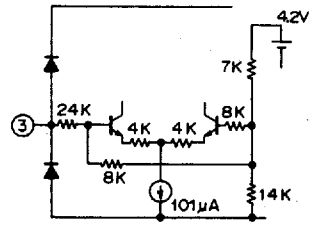
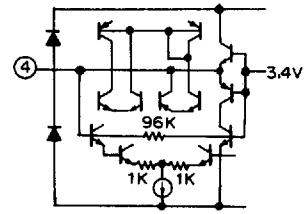
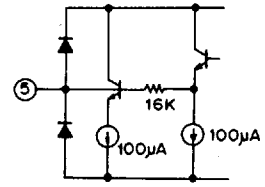
Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	BPF F0	2.1V		Filter fo adjustment. The current derived from this pin is made variable for filter fo adjustment.
2	HUE ADJ	2.0V		Hue adjustment. Applying a voltage of 0 to 5V to this pin provides hue adjustment over ± 20°.
3	CCONT	2.8V typ.		Chroma amplifier gain adjustment. Chroma amplifier adjustment is made according to the voltage applied to this pin.
4	APC TC	3.4V		APC (color sync) time constant and free-running frequency adjustment. The VXO free-running frequency is adjusted by varying the DC voltage applied to this pin.
5	VXO2	2.8V		Crystal oscillation.

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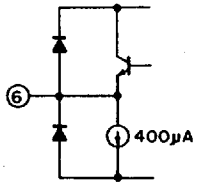
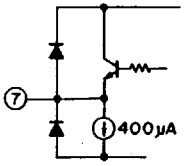
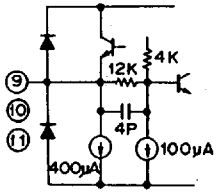
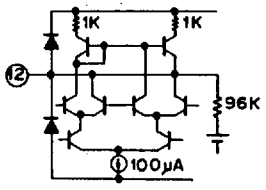
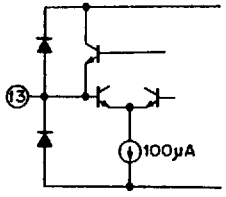
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	VXO1	3.3V		Crystal oscillation.
7	SC OUT	1.3V		Subcarrier output.
8	GND1	0V		Filter/chroma GND.
9	R	2.0V		R output.
10	G			G output.
11	B			B output.
12	ACK TC	3.2V		ACK (automatic color killer) time constant.
13	ACC TC			ACC (automatic color control) time constant.
14	GND2	0V		Y GND.

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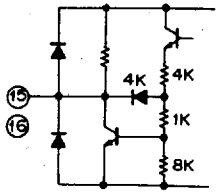
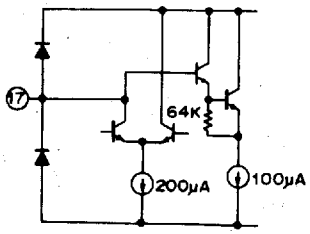
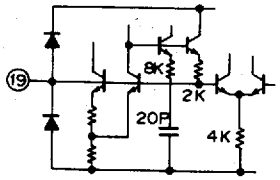
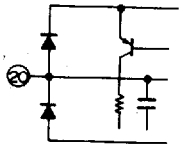
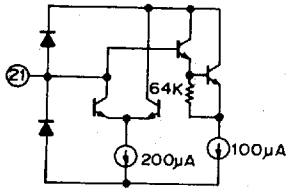
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	CSYNC	H; 2.4V min. L; 0.4V max.		Composite sync output (TTL level).
16	BF			Burst flag output (TTL level).
17	TC1			Feedback clamp time constant for SYNC SEP.
18	Vcc2	5V *		Y power supply.
19	TP ADJ	1.23V		Burst flag adjustment. The burst flag position to (BF) is adjusted to 5.6 µs by varying the current derived from this pin.
20	VREG	4.2V		4.2V regulator output. It provides a decoupling capacity.
21	CLP TC			Pedestal clamp time constant.

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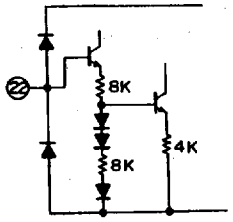
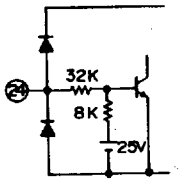
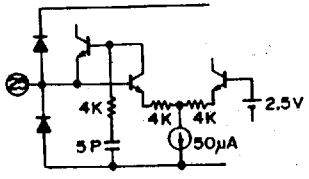
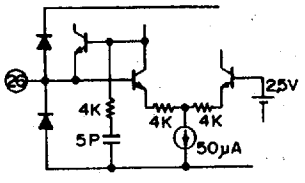
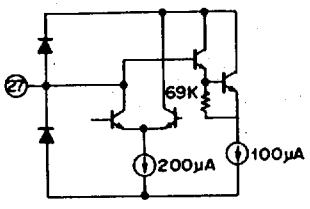
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
22	APL CTL	2.5V		APL sensitivity adjustment. When the APL amplifier is not required, connect this pin to the GND.
23	Vcc1	5V		Filter/chroma power supply.
24	SHP CTL	2.5V		(1) Sharpness gain adjustment. (2) Variable range: –5dB to +5dB ($1.5 \leqq V_{24} \leqq 3.5$). (3) The fo band gain can be adjusted by varying the voltage applied to this pin.
25	SHP FO	2.1V		Filter frequency adjustment. Filter fo adjustment is made by varying the current derived from this pin.
26	DL FO	2.1V		Delay line delay amount adjustment. The delay amount is adjusted by varying the current derived from this pin.
27	APL TC	2.0V		Time constant for luminance signal APL (average picture level) detection.

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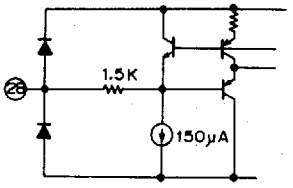
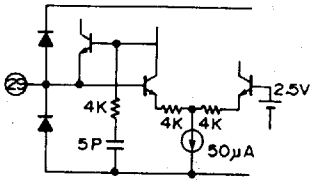
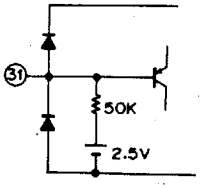
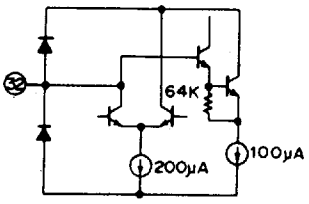
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	TRAP OUT	2.5V		The Y signal passing through the trap can be monitored at this pin. To obtain a deeper trap, connect the LC in series with the GND.
29	TRAP FO	2.1V		Filter fo adjustment. Filter fo adjustment is made by varying the current derived from this pin.
30	NC			
31	COMP IN	2.5V		Composite video signal input. Typical input is 0.56Vp-p.
32	CLP2 TC			Pedestal clamp time constant.

Electrical Characteristics

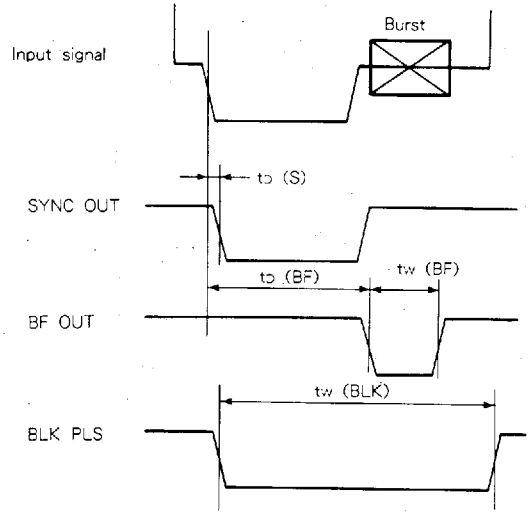
(Ta=25°C, Vcc=5V, See the electrical characteristics test circuit.)

Test item		Symbol	Conditions		Input signal	Test point	Min.	Typ.	Max.	Unit
Current consumption 1		Icc1			1	A1	17.0	26.5	36.5	mA
YAMP voltage gain		Vo (R)	V_{DC}=200mV V_{AC}=160mVp-p F_{AC}=300kHz See detailed test procedure 1.		2	V1	6.5	8	9.5	dB
		Vo (G)				V2				
		Vo (B)				V3				
YAMP frequency response characteristics		Fc (R)	Input frequency required for –3dB output generation when the output at 300kHz is 0dB SHP FO (external 39kΩ) SHP CTL=2.5V		2	V1	1.8			MHz
		Fc (G)				V2				
		Fc (B)				V3				
Trap attenuation		V_{TP}	V_{DC}=200mV V_{AC}=160mVp-p F_{AC}=3.58MHz * Ratio of the output at 3.58MHz to the 0dB output at 300kHz		2	V3			–30	dB
Sharpness characteristics	MAX	V_{SHP} (MAX)	V_{DC}=280mV V_{AC}=160mVp-p V_{FC}=1.5MHz * Ratio of the output at 1.5MHz to the 0dB output at 300kHz	SHP CTL =3.5V	2	V3	5.0			dB
	MIN	V_{SHP} (MIN)		SHP CTL =1.5V	2	V3			–5.0	dB
AGC characteristics	20% white	V_{AGC1}	V_{DC}=80mV V_{AC}=60mVp-p F_{AC}=300kHz APL CTL=2.5V		2	V3	4.3	6	7.0	dB
	50% white	V_{AGC2}	V_{DC}=200mV V_{AC}=160mVp-p F_{AC}=300kHz APL CTL=2.5V		2	V3	3.3	4.6	5.8	
	100% white	V_{AGC3}	V_{DC}=400mV V_{AC}=160mVp-p F_{AC}=300kHz APL CTL=2.5V		2	V3	1.3	2.5	3.5	
Demodulated output DC voltage		E_{ODC} (R)			1	V1	1.5		2.7	V
		E_{ODC} (G)				V2				
		E_{ODC} (B)				V3				
Primary color output voltage		Eo (R)	See detailed test procedure 2.		3	V1	1.1			Vp-p
		Eo (G)				V2				
		Eo (B)				V3				
Demodulated output residual carrier		C_L (R)	3.58MHz component of the output		1	V1			20	mV
		C_L (G)				V2				
		C_L(B)				V3				
ACC characteristic 1		Acc1	$Acc1 = \frac{Voc(Vin=-14dB)}{Voc(Vin=0dB)}$		3	V3	–4			dB
ACC characteristic 2		Acc2	$Acc2 = \frac{Voc(Vin=+6dB)}{Voc(Vin=0dB)}$		3	V3			3	dB
Color killer level		Ek	Chroma input level during color operation		3	V3	–55		–33	dB
APC pull-in		Fp			5	F1	±250			Hz

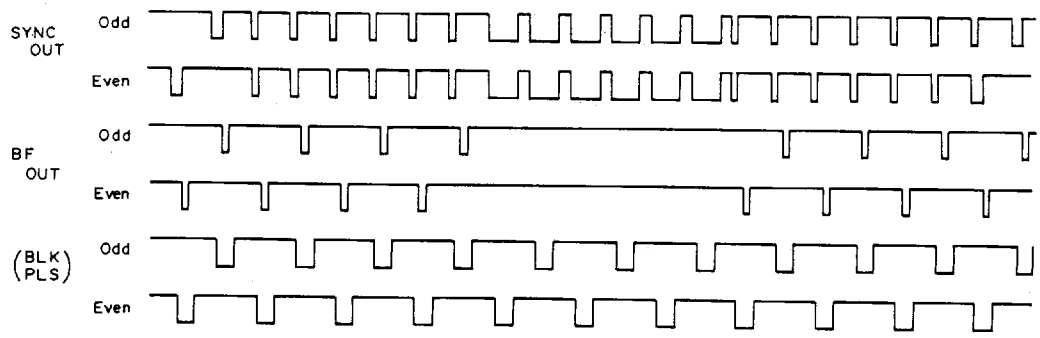
Test item		Symbol	Conditions	Input signal	Test point	Min.	Typ.	Max.	Unit
Sync output	H level	V_{OH} (S)		1	V4	2.4			V
	L level	V_{OL} (S)						0.4	
	Delay time	t_D (S)					0.5		µs
Burst flag output	H level	V_{OH} (BF)		1	V5	2.4			V
	L level	V_{OL} (BF)		1	V5			0.4	V
	Pulse width	tw (BF)	When the t_D (BF) value is adjusted to 5.6 µs	1	V5		2.4		µS
Blanking pulse width		tw (BLK)		4	V3	7.5	9.2	11.0	µS

Sync System Timing Chart

H sync



V sync NTSC



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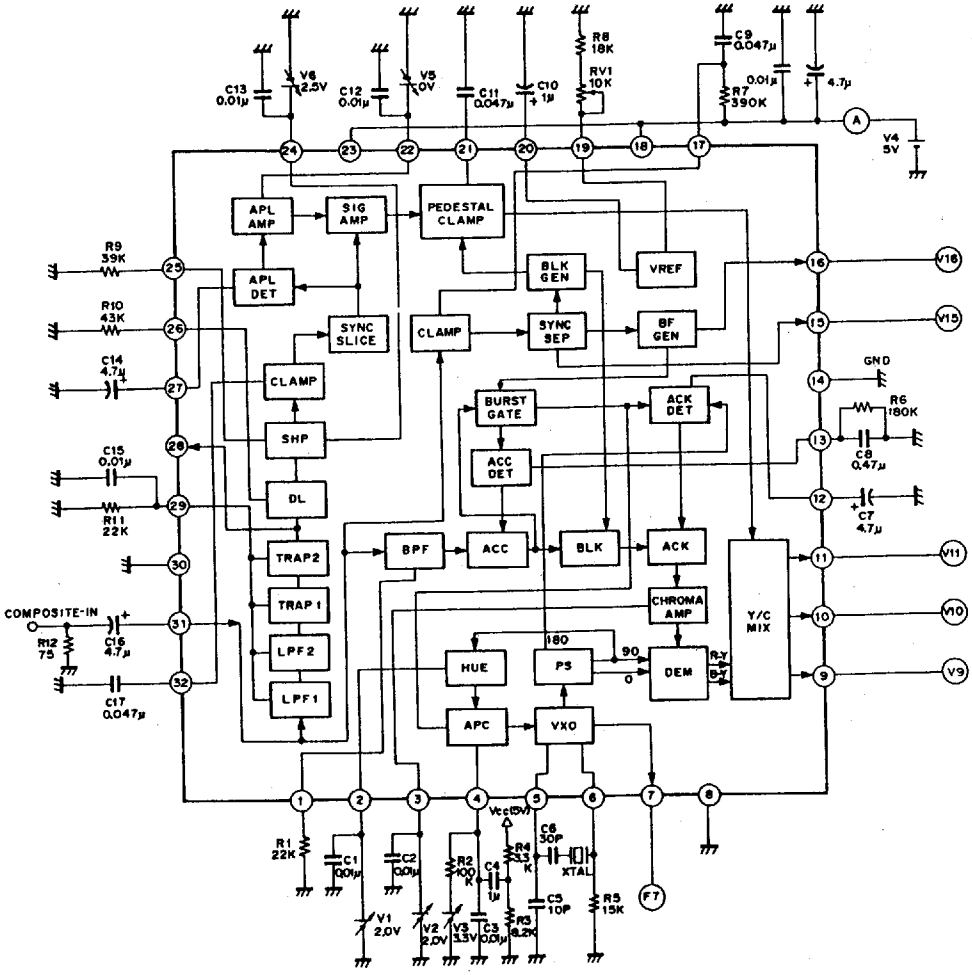
Electrical Characteristics Test Circuit



Note) Unless otherwise specified in the Conditions column of the electrical characteristics, the above indicated values are to be applied to V_1, V_2, V_3, V_5, and V_6.

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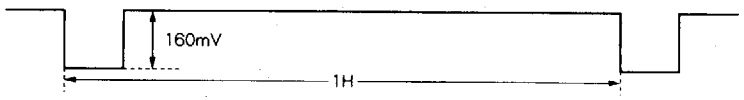
Input Signals

1



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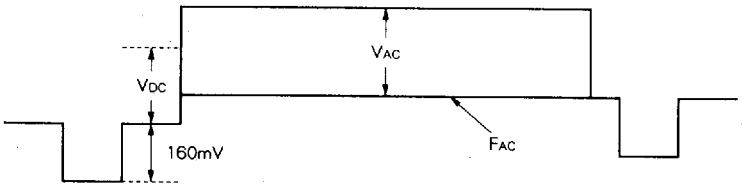
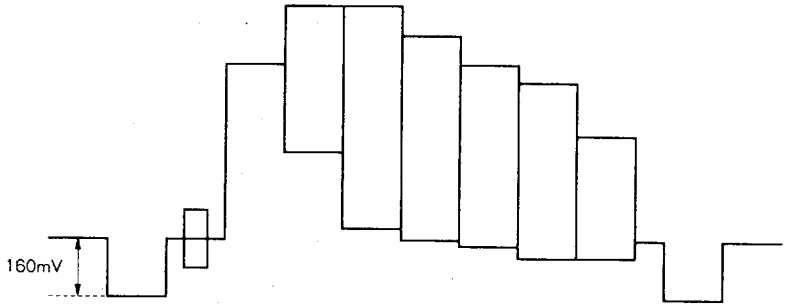
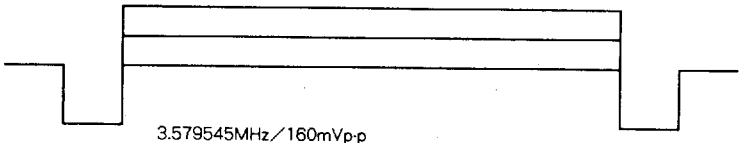


3

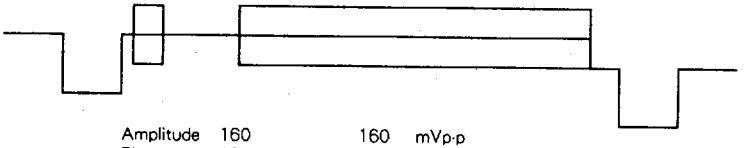


Luminance level	0,	300,	268,	212,	176,	124,	88,	32,	0, mV
Amplitude	160,	0,	264,	376,	352,	352,	376,	264,	0, mVp-p
Phase	180,	–	168,	284,	241,	61,	104,	348,	–, deg
Frequency	3.579545MHz								

4



5



Amplitude	160	160	mVp-p
Phase	180	0	deg
Frequency	3.579545MHz ± 250Hz		

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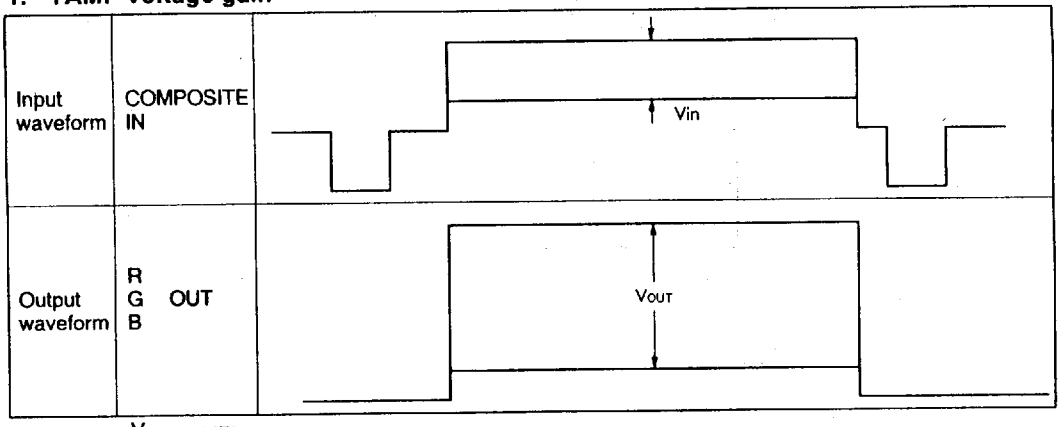
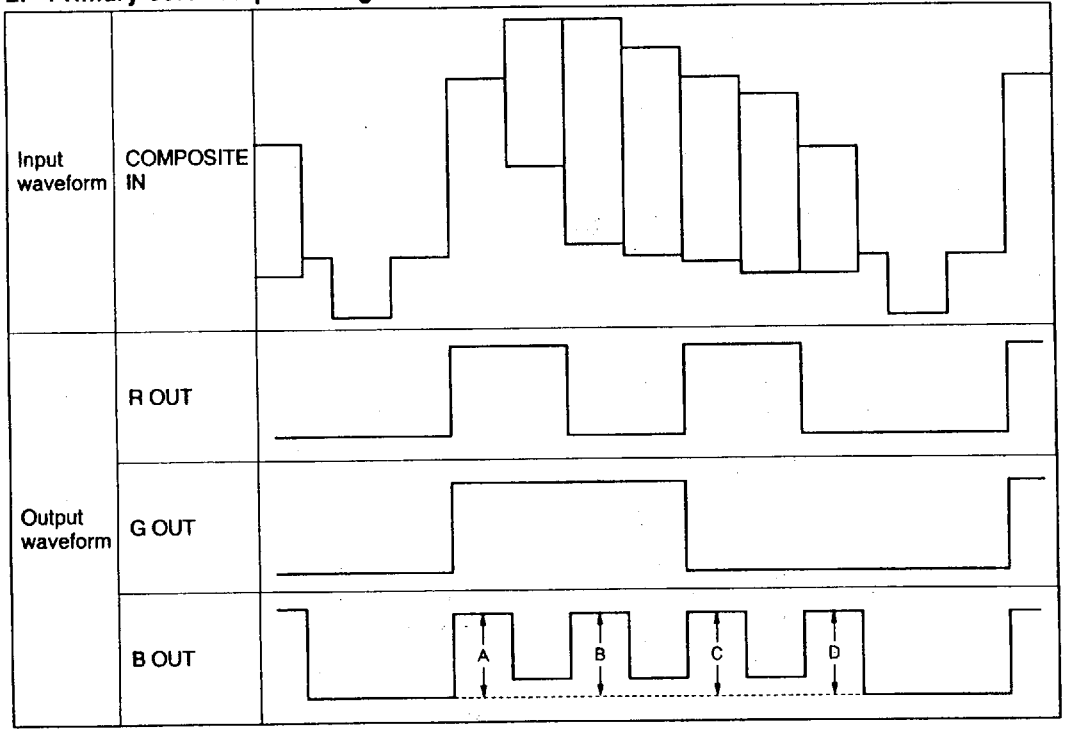
Detailed Test Procedures

1. YAMP voltage gain



$G=20\log \frac{V_{OUT}}{Vin}$ (dB)

2. Primary color output voltage



Adjustment Procedure (Input signal: 75% color-bar)

1. Adjust the HUE ADJ and C CONT controls so that B output amplitudes A, B, C, and D are equal.

Application Circuit

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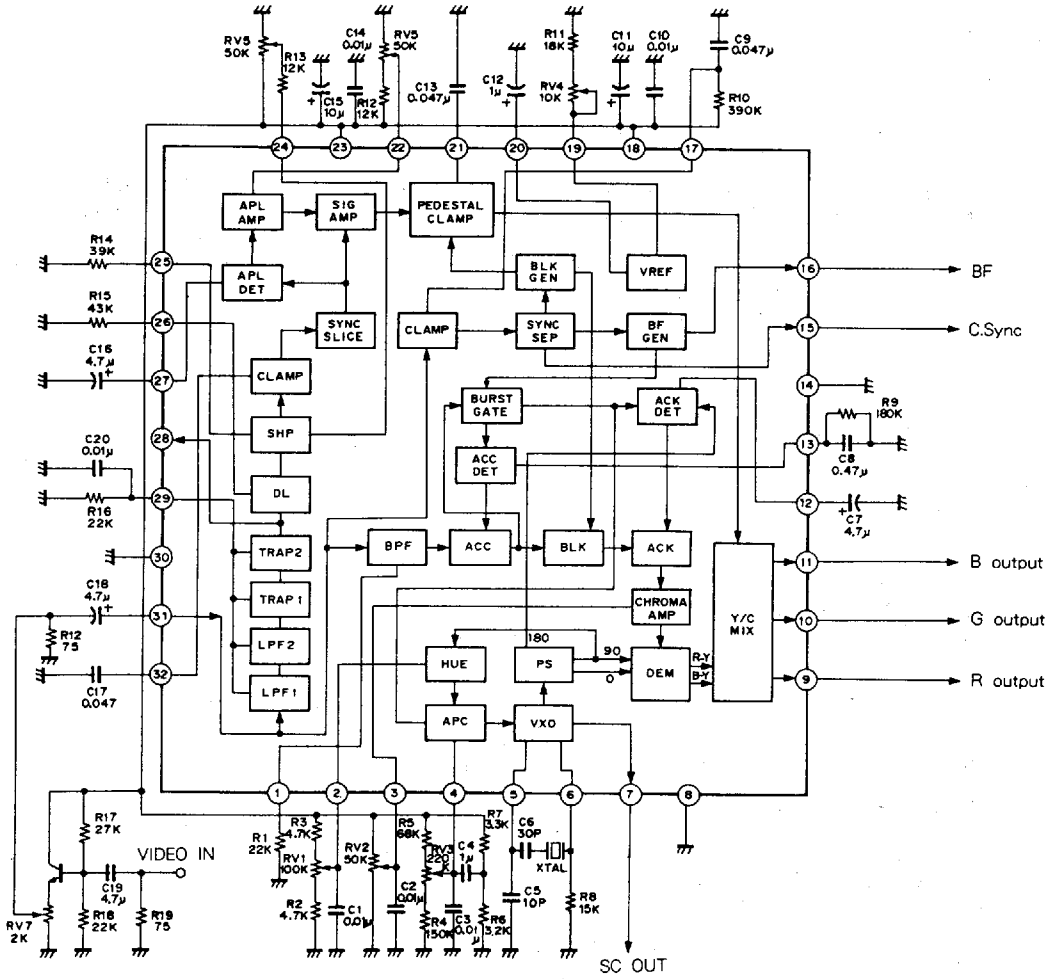

* Change the C19 input capacitor polarity in accordance with the operating conditions.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

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Description of Operation

(1) Luminance Signal Regeneration System

i) Trap Filters
Two LPFs and two trap filters are used to derive the luminance signal from the composite signal.

ii) Delay Line Filter
Makes delay amount adjustment relative to the color signal.

iii) Sharpness Filter
Accentuates the 1.5MHz region of the luminance signal passing through the delay line. The voltage applied to Pin 24 (SHP CTL) varies the 1.5MHz component over the range from –5 to +5dB (with reference to 300kHz). When 2.5V is applied to Pin 24 (SHP CTL), the 0dB level (with reference to 300kHz) results.

iv) APL Circuit
The APL (average picture level) is used to control the YAMP gain. When the APL is low, the gain is increased. When the APL is high, on the other hand, the gain is decreased. The AGC turns ON when 2.5V is present at Pin 22 (APL CTL). If the AGC function is not needed, the AGC circuit is turned OFF by applying 0V to Pin 22.

(2) Color Signal Regeneration System

i) BPF
Derives the chroma signal from the composite signal.

ii) ACC Circuit
After the chroma signal is passed through the BPF, the burst signal is detected by the ACC DET. The feedback resulting from detection is then returned to the ACC AMP so as to maintain the burst level constant.

iii) APC Circuit
After being adjusted to a fixed level by the ACC AMP, the signal passes through the burst gate circuit so that only the burst signal enters the APC circuit. Meanwhile, the VXO output is fed to the phase circuit, where the 0 °, 90 °, and 180 ° signals are generated. These signals then go into the hue circuit, and the resultant synthesized signal (90 ° carrier) enters the APC circuit. The phase of this signal is compared against that of the burst signal, and a feedback signal is transmitted to the VXO so that a phase difference of 90 ° occurs. The 0 ° and 90 ° carriers generated in this manner are supplied to the B–Y and R–Y DEM sections. Therefore, the DC voltage applied to Pin 2 (HUE ADJ) controls the synthesized wave phase to vary the demodulation axis.

iv) DEM Circuit
After being adjusted to a fixed level by the ACC AMP, the chroma signal is amplified by the CHROMA AMP, demodulated by the B–Y DEM and R–Y DEM, fed to the Y/C MIX circuit together with the G–Y signal generated by the resistor matrix, and mixed with the luminance signal to generate the R, G, and B primary color outputs.

(3) Sync Separation System

After the composite video signal is entered via Pin 31 (COMP IN), the sync tip is clamped so that sync separation occurs. The resulting SYNC pulse is used to generate the BF (burst flag), BLK, and other timing pulses to be supplied to various circuits. The SYNC and BF pulses are converted to TTL level through buffer, and transferred out.

Adjustment Procedures

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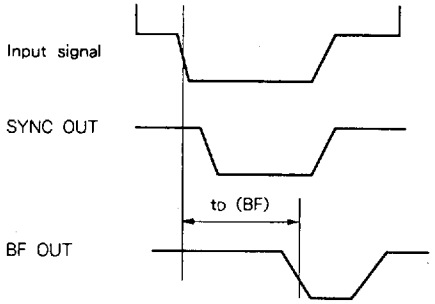
Input signal: 75% color-bar (NTSC)

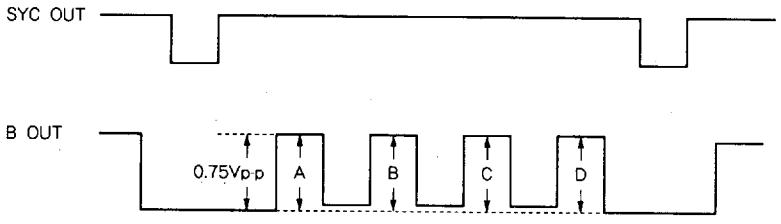
1) fo adjustment
Adjust the Pin 4 (APC TC) DC voltage so that the Pin 7 (SCOUT) oscillation frequency (subcarrier output) is within fsc (=3.579545MHz) ± 20Hz in a no-signal state (free-run).

2) BF position adjustment
Adjust the resistance between Pin 19 and GND to set the BF (burst flag) position to (BF) to 5.6 µs.



3) Input level adjustment
With Pin 22 (APL CTL) connected to the GND, adjust the input level so that the B output white peak (75% white) is 0.75Vp-p.

4) HUE ADJ and C CONT adjustments
Adjust the HUE ADJ and C CONT controls so that the amplitudes of all B output colors (A, B, C, and D below) are equal.



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Application

1. The maximum input dynamic range is 0.56Vp-p.
   The details are given below.

Composite video signal	0.56Vp-p
Sync signal	0.16Vp-p
Luminance signal	0.40Vp-p (100% white)
Burst signal	0.16Vp-p

   The value 0.56Vp-p is measured from the sync tip to the white peak. Note that the output may be clipped and distorted if the input signal is greater than 0.56Vp-p.
   However, this applies when the AGC is OFF (Pin 22 [APL CTL]=0V).

2. Filter F0 pin
   The filter F0 sensitivities are as follows.

BPF F0	−150kHz/+kΩ
TRAP F0	−140kHz/+kΩ
SHARP F0	−40kHz/+kΩ
DELAY F0	+4nS/+kΩ

3. To obtain a deeper trap, connect the LC (100 μH, 20 pF) in series between Pin 28 (TRAP OUT) and GND. The trap is then rendered about 3dB deeper.

4. Notes on operation

   i) When making wiring connections, ensure that Pin 28 (TRAP OUT) is not affected by signal input or X'tal (crystal oscillator) oscillation frequency.

   ii) The fo value of the X'tal varies with the floating capacity and other factors. Therefore, mount the X'tal as close as possible to the IC using a minimum of connecting wiring.

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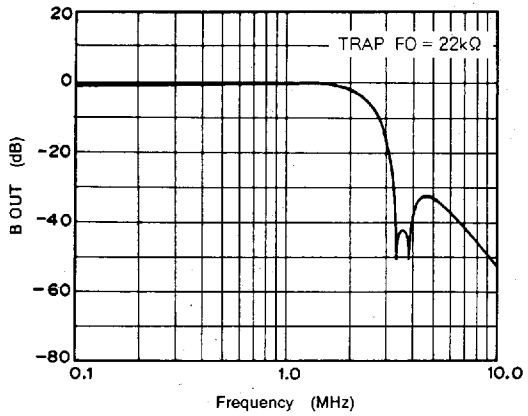
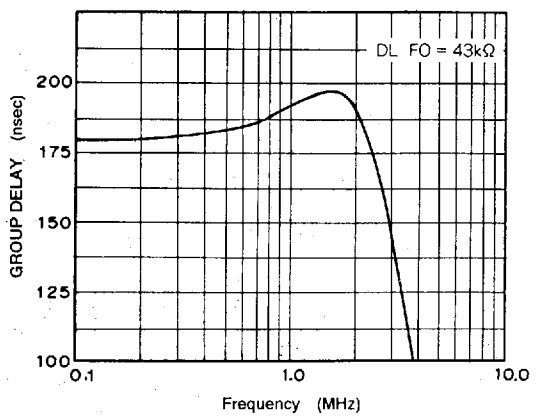
Example of Representative Characteristics

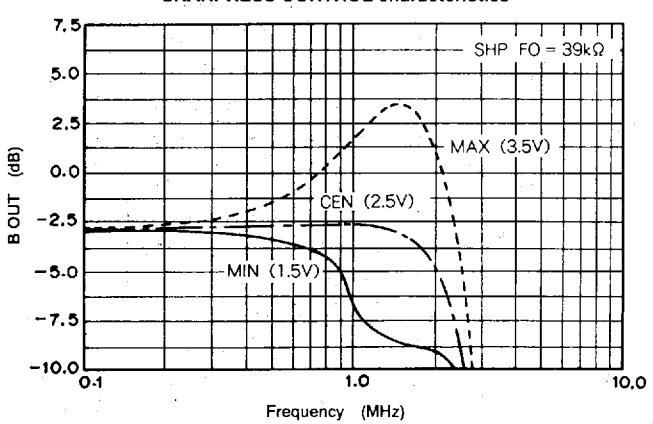
TRAP characteristics



DELAY characteristics



SHARPNESS CONTROL characteristics



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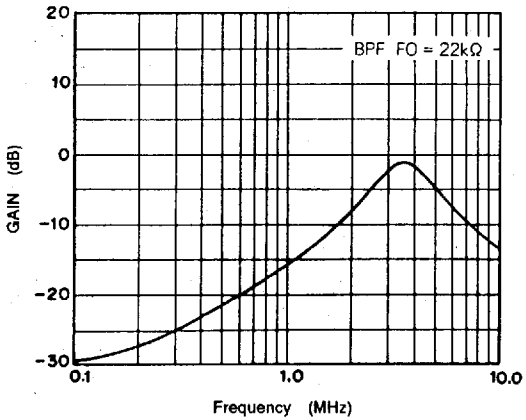
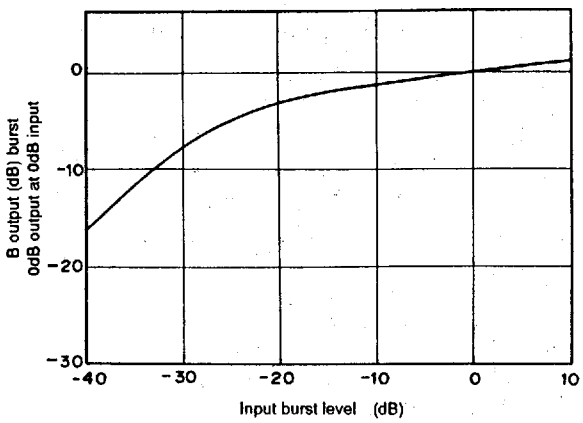
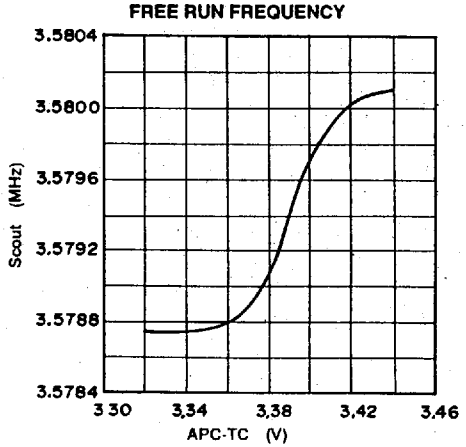
BPF characteristics



ACC characteristics



FREE RUN FREQUENCY



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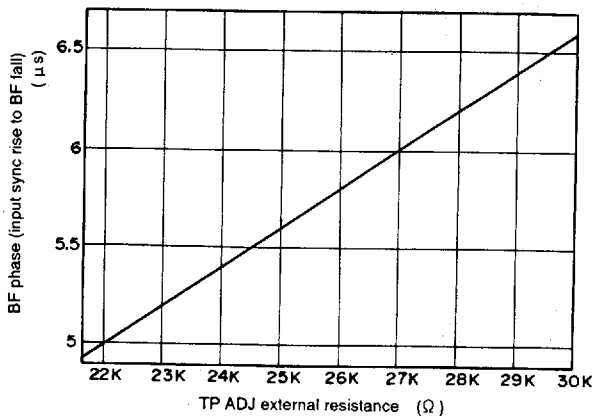
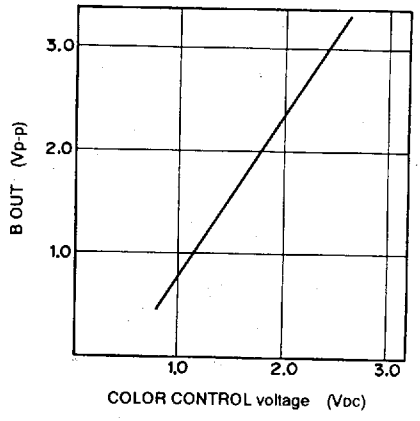
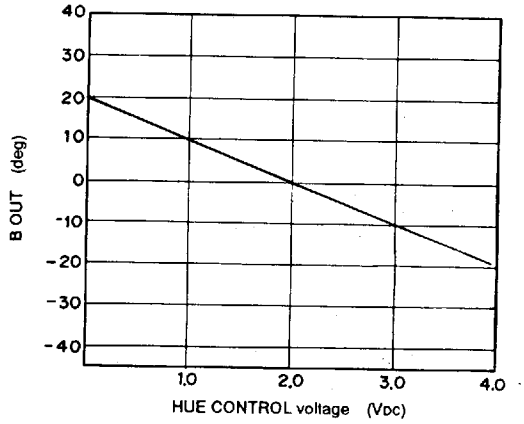
BF phase characteristics provided by TD ADJ (external resistor)



Color control characteristics



Hue control characteristics



Package Outline Unit : mm

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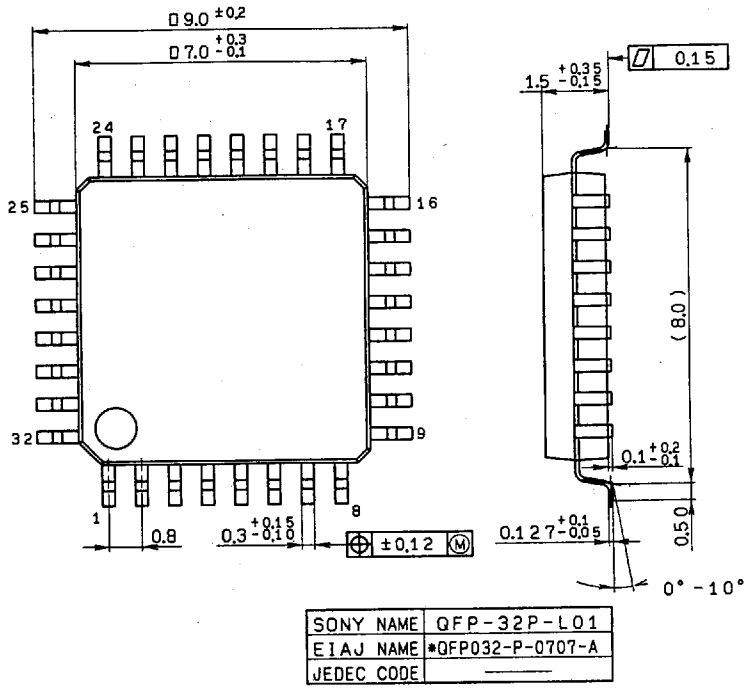
32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———